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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/295,607	04/22/1999	SHUNPEI YAMAZAKI	0756-1961	7371

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EXAMINER
LOKE, STEVEN HO YIN

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/295,607	Applicant(s) YAMAZAKI ET AL.	
	Examiner Steven Loke	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,6-8,11,12,15-17,19-35 and 37-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,6-8,11,12,15-17,19-35 and 37-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *33, 34* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. Claims 43-53, 55, 58, 61,63, 65 and 67 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification never discloses a layer comprising silicon nitride on the channel formation region as claimed in claims 43-53, 55 and 58.

The specification never discloses a pixel electrode over the transistor as claimed in claim 61.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 60-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Troxell et al. in view of Ikeda (Japanese patent no. 59-121876 in PTO-1449), further in view of Shimada et al.

In regards to claims 60 and 61, Troxell et al. discloses a semiconductor device in fig. 1. It comprises: a polycrystalline silicon thin film transistor formed on a glass substrate [10]; a silicon nitride layer [14] and silicon dioxide layer [16] formed on the top surface of the glass substrate [10] and a silicon nitride layer [12] formed on the bottom surface of the glass substrate [10].

Troxell et al. differs from the claimed invention by not showing an AlN layer formed on the rear surface and the top surface of the substrate.

Ikeda shows an AlN layer [12] formed on the rear surface and the top surface of a glass substrate [11] in fig. 1(c).

Since both Troxell et al. and Ikeda teach an insulating layer formed on a glass substrate, it would have been obvious to have the AlN layer of Ikeda formed on the rear surface and the top surface of the glass substrate of Troxell et al. because they prevent a thin film device from deforming at the time of forming the device. The combined device shows a composite insulating film comprising AlN and oxygen provided over the front surface of the glass substrate.

Troxell et al. further differs from the claimed invention by not showing a pixel electrode over the leveled interlayer insulating film.

Shimada et al. discloses a semiconductor device in figs. 1-3. It comprises: a polycrystalline silicon thin film transistor formed on a glass substrate [11]; the thin film transistor having a channel formation region comprising crystalline silicon, a gate insulating film [13] adjacent to the channel formation region, and a gate electrode [3a] adjacent to the channel formation region with the gate insulating film interposed therebetween; an interlayer insulating film [17] having a leveled upper surface over the transistor; a pixel electrode [4] over the interlayer insulating film [17].

Since both Troxell et al. and Shimada et al. teach an insulated gate field effect transistor serves as pixel control switch in the liquid crystal display, it would also have been obvious to have the interlayer insulating film and the pixel electrode of Shimada et

al. in Troxell et al. because the interlayer insulating film can protect the transistor and the pixel electrode can provide an image from the transistor.

In regards to claims 62, 63, the combined device discloses a glass substrate.

In regards to claims 66, 67, the combined device shows the insulating AlN layer has an aluminum to nitrogen ratio of 1.0.

In regards to claims 64, 65, it is well known in the semiconductor art that aluminum nitride has a thermal conductivity of 0.6 W/cm K or higher.

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 2, 3, 6, 7, 8, 11, 12, 15-17, 19, 20, 22-26, 28-35, 37, 38, 40-49 and 51-53 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15-26 of U.S. Patent No. 5,583,369 (Yamazaki et al.) in view of Troxell et al.

Yamazaki et al. discloses a SOI device in fig. 12(E). It comprises: an AlN layer [1102] containing at least one of boron, silicon, carbon and oxygen formed on a top

surface and a bottom surface of a glass substrate [1101]; an oxide layer [1103] formed on the AlN layer [1102]; an insulated gate field effect transistor formed on the substrate.

Yamazaki et al. differs from the claimed invention by not showing the channel region comprising crystalline silicon.

Troxell et al. discloses a semiconductor device in fig. 1. It comprises: a polycrystalline silicon thin film transistor formed on a glass substrate [10].

Since both Yamazaki et al. and Troxell et al. teach an insulated gate field effect transistor formed on a glass substrate, it would have been obvious to have the transistor of Troxell et al. in Yamazaki et al. because it is a widely used thin film transistor structure.

In regards to claims 3, 7, 20, it is well known in the semiconductor art that aluminum nitride has a thermal conductivity of 0.6 W/cm K or higher.

In regards to claims 22-24, Ikeda shows the insulating AlN layer [12] has an aluminum to nitrogen ratio of 1.0.

In regards to claims 43-49, 51-53, Troxell et al. shows a silicon dioxide layer [28] formed on the polycrystalline silicon layer [20] in fig. 1.

In regards to claims 43-49, 51-53, the process limitation of how the channel formation region is formed has no patentable weight in claim drawn to structure. It is important to note that there are many ways to form the channel formation region. Therefore, the phrase "crystallized by laser irradiation through a layer comprising at least one of silicon oxide and silicon nitride" is thus non-limiting.

6. Claims 21, 27, 39 and 50 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15-26 of U.S. Patent No. 5,583,369 (Yamazaki et al.) in view of Mano et al.

Yamazaki et al. discloses a SOI device in fig. 12(E). It comprises: an AlN layer [1102] containing at least one of boron, silicon, carbon and oxygen formed on a top surface and a bottom surface of a glass substrate [1101]; an oxide layer [1103] formed on the AlN layer [1102]; an insulated gate field effect transistor formed on the substrate.

Yamazaki et al. differs from the claimed invention by not showing the channel region comprising crystalline silicon.

Mano et al. discloses a semiconductor device in fig. 7. It comprises: a polycrystalline silicon thin film transistor formed on a quartz substrate [408].

Since both Yamazaki et al. and Mano et al. teach an insulated gate field effect transistor formed on a substrate, it would have been obvious to have the transistor of Mano et al. in Yamazaki et al. because it is a widely used thin film transistor structure.

In regards to claims 45, 50, Mano et al. shows a silicon oxide gate insulating film [412] formed on the polycrystalline silicon [409] in fig. 7.

In regards to claims 45, 50, the process limitation of how the channel formation region is formed has no patentable weight in claim drawn to structure. It is important to note that there are many ways to form the channel formation region. Therefore, the phrase "crystallized by laser irradiation through a layer comprising at least one of silicon oxide and silicon nitride" is thus non-limiting.

7. Claims 54-67 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15-26 of U.S. Patent No. 5,583,369 (Yamazaki et al.) in view of Shimada et al.

Yamazaki et al. discloses a SOI device in fig. 12(E). It comprises: an AlN layer [1102] containing at least one of boron, silicon, carbon and oxygen formed on a top surface and a bottom surface of a glass substrate [1101]; an oxide layer [1103] formed on the AlN layer [1102]; an insulated gate field effect transistor formed on the substrate.

Yamazaki et al. differs from the claimed invention by not showing the channel region comprising crystalline silicon, and an interlayer insulating film having a leveled upper surface over the transistor and a pixel electrode over the interlayer insulating film.

Shimada et al. discloses a semiconductor device in figs. 1-3. It comprises: a polycrystalline silicon thin film transistor formed on a glass substrate [11]; the thin film transistor having a channel formation region comprising crystalline silicon, a gate insulating film [13] adjacent to the channel formation region, and a gate electrode [3a] adjacent to the channel formation region with the gate insulating film interposed therebetween; an interlayer insulating film [17] having a leveled upper surface over the transistor; a pixel electrode [4] over the interlayer insulating film [17].

Since both Yamazaki et al. and Shimada et al. teach an insulated gate field effect transistor formed on a substrate, it would have been obvious to have the transistor of Shimada et al. in Yamazaki et al. because it is a widely used thin film transistor structure. It would also have been obvious to have the interlayer insulating film and the pixel electrode of Shimada et al. in Yamazaki et al. because the interlayer insulating film

can protect the transistor and the pixel electrode can provide an image from the transistor.

In regard to claims 55, 58, Shimada et al. shows a silicon oxide gate insulating film [13] formed on the polysilicon layer [12] in figs. 1-3.

In regards to claims 55, 58, the process limitation of how the channel formation region is formed has no patentable weight in claim drawn to structure. It is important to note that there are many ways to form the channel formation region. Therefore, the phrase "crystallized by laser irradiation through a layer comprising at least one of silicon oxide and silicon nitride" is thus non-limiting.

In regards to claims 64, 65, it is well known in the semiconductor art that aluminum nitride has a thermal conductivity of 0.6 W/cmK or higher.

8. Applicant's arguments filed 5/16/02 have been fully considered but they are not persuasive.

It is urged, in page 3 of the remarks, that the feature of "a pixel electrode over the transistor" recited in claim 61 is supported by Figs. 10(D) and (E) and in page 40, third paragraph, of the specification. However, Figs. 10(D) and (E) show the pixel electrode [213] over the insulating layer [212] instead of the transistor. The specification (page 40, third paragraph) never discloses a pixel electrode over the transistor.

It is urged, in pages 4-5 of the remarks, that none of the references cited by the Examiner discloses insulating film comprises oxygen or carbon and aluminum nitride comprising oxygen or carbon. However, the combined device of Troxell et al., Ikeda and Shimada et al. shows a composite insulating film comprising AlN and oxygen

provided over the front surface of the glass substrate. Since claims 15-26 of U.S. Patent No. 5,583,369 (Yamazaki et al.) show an AlN layer [1102] containing at least one of boron, silicon, carbon and oxygen formed on a top surface and a bottom surface of a glass substrate [1101], the combined device of Yamazaki et al. and Troxell et al. discloses the claimed devices of claims 2, 3, 6, 7, 8, 11, 12, 15-17, 19, 20, 22-26, 28-35, 37, 38, 40-49 and 51-53. The combined device of Yamazaki et al. and Mano et al. discloses the claimed devices of claims 21, 27, 39 and 50. The combined device of Yamazaki et al. and Shimada et al. discloses the claimed devices of claims 54-67.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
July 27, 2002

Steven Loke
Primary Examiner